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Exhibit A



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Hansen et al.

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(54) **SYSTEM WITH WIDE OPERAND ARCHITECTURE, AND METHOD**

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This patent is subject to a terminal disclaimer.

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- (51) Int. Cl.⁷ **G06F 15/00**
(52) U.S. Cl. **712/210; 712/28; 712/24; 712/32; 712/208**
(58) Field of Search **712/32, 28, 31, 712/208, 210, 20, 24**

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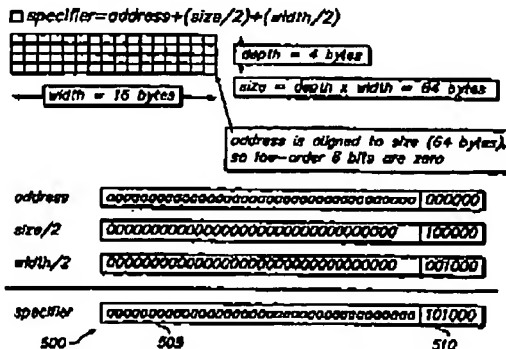
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ABSTRACT

The present invention provides a system and method for improving the performance of general purpose processors by expanding at least one source operand to a width greater than the width of either the general purpose register or the data path width. In addition, the present invention provides several classes of instructions which cannot be performed efficiently if the operands are limited to the width and accessible number of general purpose registers. The present invention provides operands which are substantially larger than the data path width of the processor by using a general purpose register to specify a memory address from which at least more than one, but typically several data path widths of data can be read. The present invention also provides for the efficient usage of a multiplier array that is fully used for high precision arithmetic, but is only partly used for other, lower precision operations.

48 Claims, 148 Drawing Sheets

Microfiche Appendix Included
(5 Microfiche, 63 Pages)



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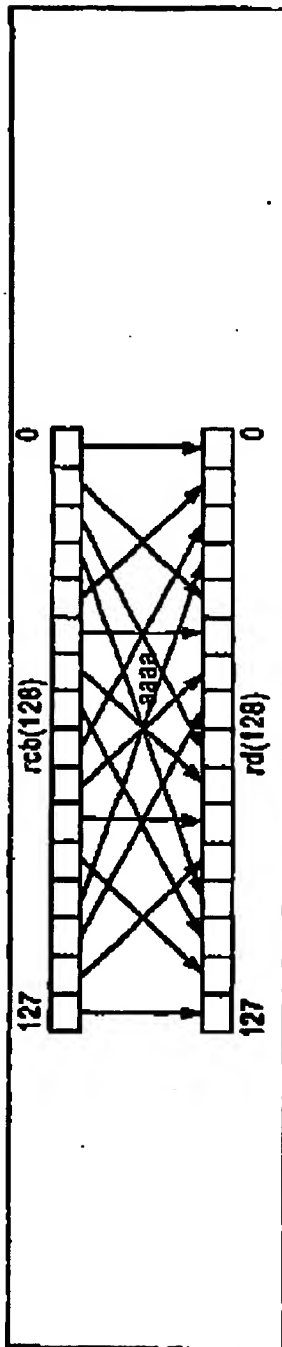
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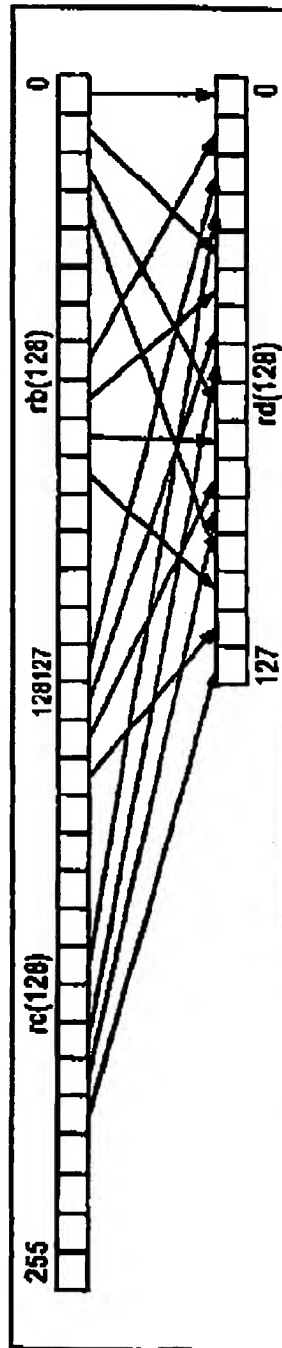
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4-way shuffle bytes within hexlet

FIG. 34D



4-way shuffle bytes within trilet

FIG. 34E